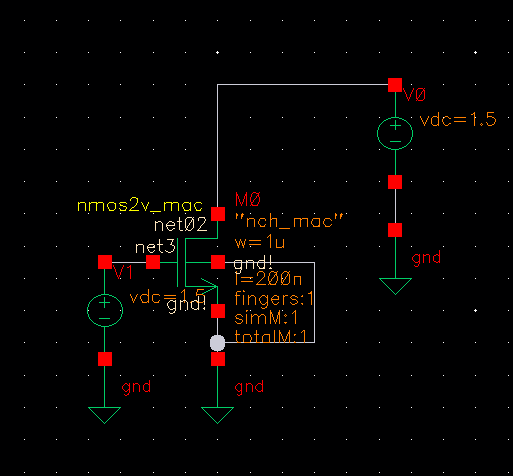
ETICD Lab#1

We have been asked to use simulations to find different parameters of a Nmos transistor and Pmos transistor, and simulate a inverter using Nmos and Pmos transistors.

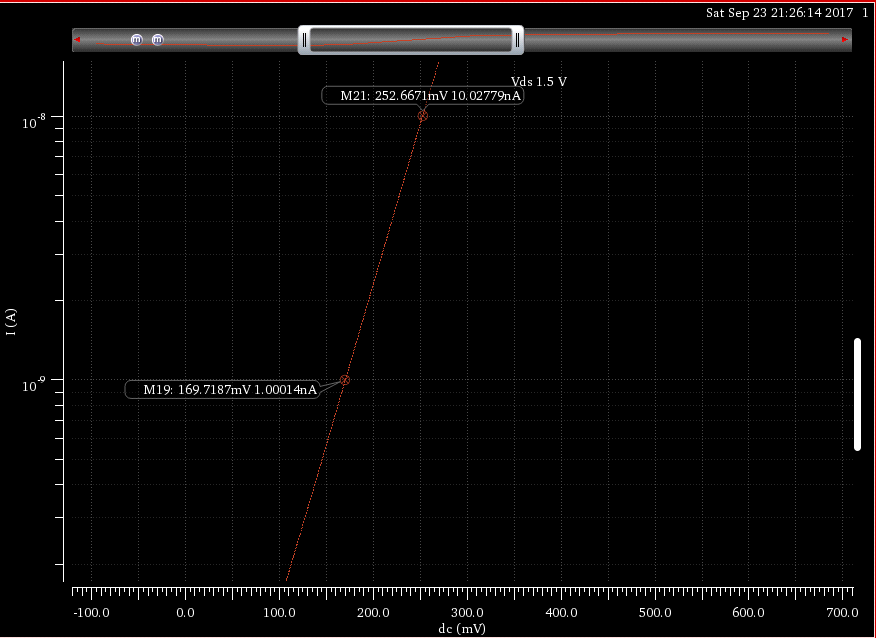
* Nmos

The Nmos transistor has to follow the following specifications; W/L=1μm/200nm and have a Vdd=1.5V. Below is the schematic of the transistor used in our simulations.



*Figur 1 NMOS test bench schematic*

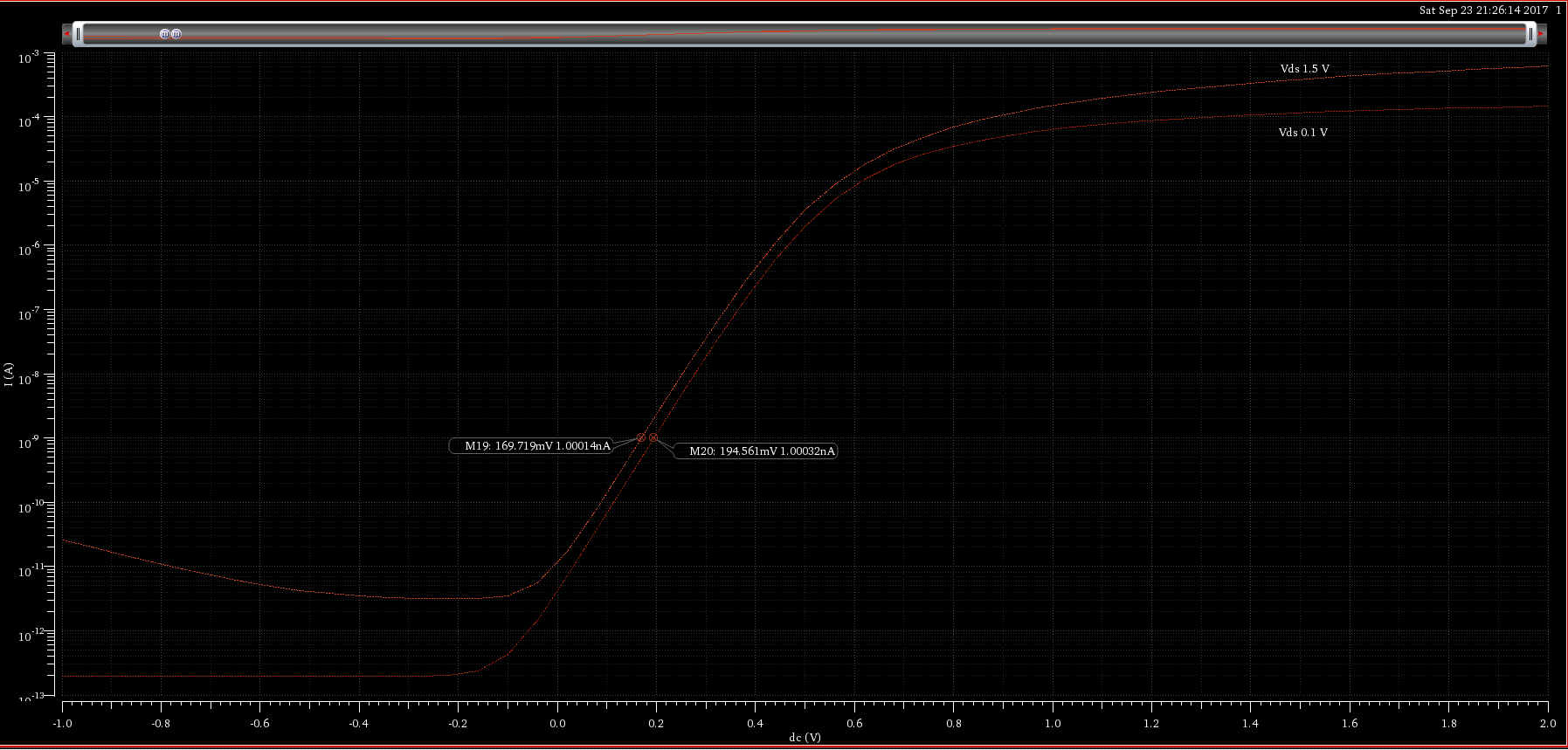
Subthreshold slope



*Figur 3 Subthreshold slope of the NMOS transistor*

The subthreshold slope is fund be looking at the graph (Figur 2) in the subthreshold region where Vgs < Vth. To find the subthreshold you can measure the voltage difference between two decades. So, for our simulation the subthreshold slope is 252mV-169mV = 83mV/decade. The typical subthreshold at room temperature is around 60mV/decade.

DIBL



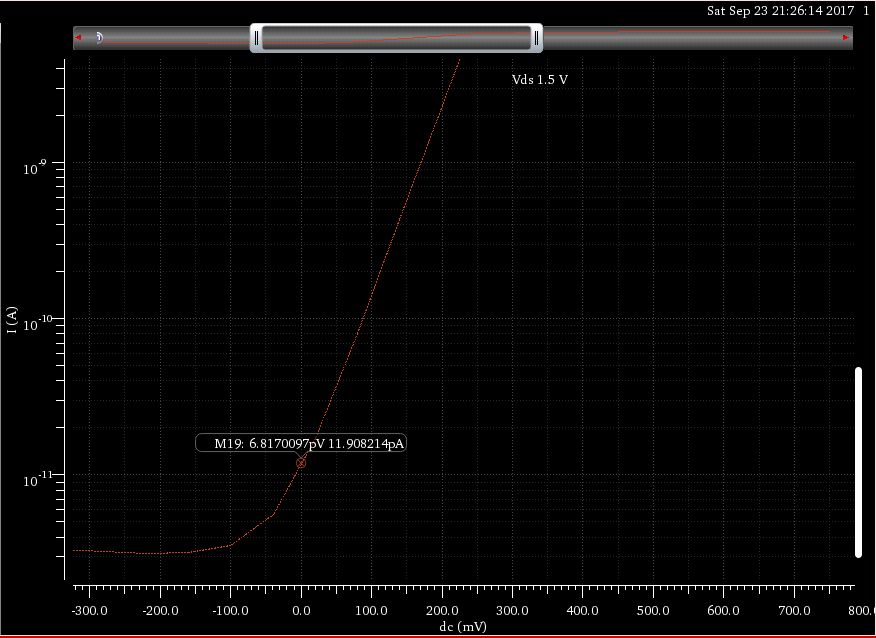
*Figur 4 DIBL of the NMOS transistor with markers for the two threshold voltages*

The DIBL(Drain-Induced Barrier Lowering) increases the drain source voltage leakage in transistors with short channels at low Vds voltage. By lowering the Vds voltage on the transistor and plot sweep on the same graph as your normal Vds. You can find the delta Vth and delta Vds and calculate the DIBL effect be this formula . For our transistor (see Figur 3), the DIBL is

|  |  |  |
| --- | --- | --- |
|  |  |  |

*Ligningen løses for DIBL vha. CAS-værktøjet WordMat.*

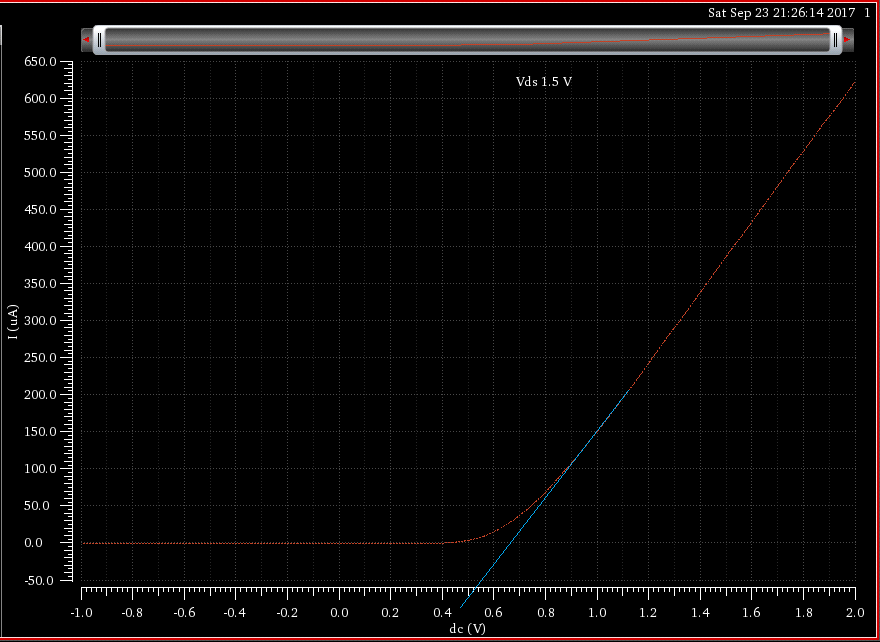
Ioff



*Figur 5 Ioff shown on the graph*

The Ioff is the current leakage from drain to source when the gate voltage is equal to zero and the NMOS transistor is turned off. As seen in Figur 4 the Ioff for our simulated NMOS transistor is ~12pA.

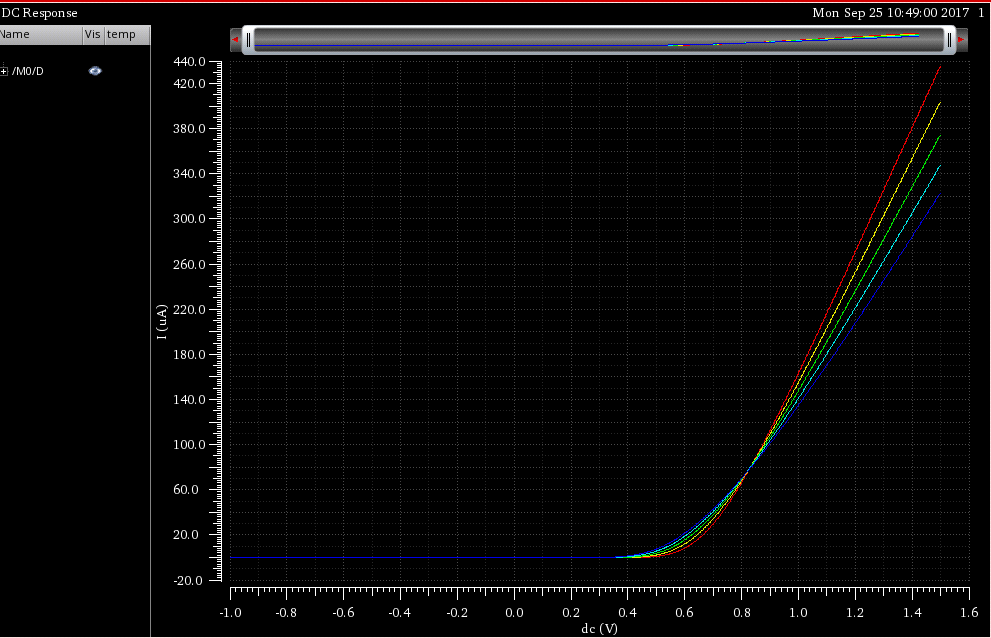
Threshold Voltage



*Figur 6 Threshold voltage of the NMOS transistor*

To read a transistor threshold voltage from a linear graph. you draw a line from the straight part of the graph as seen on Figur 5. Where the line crosses the x axis you have your threshold voltage. In our case the Vth is ~539mV.

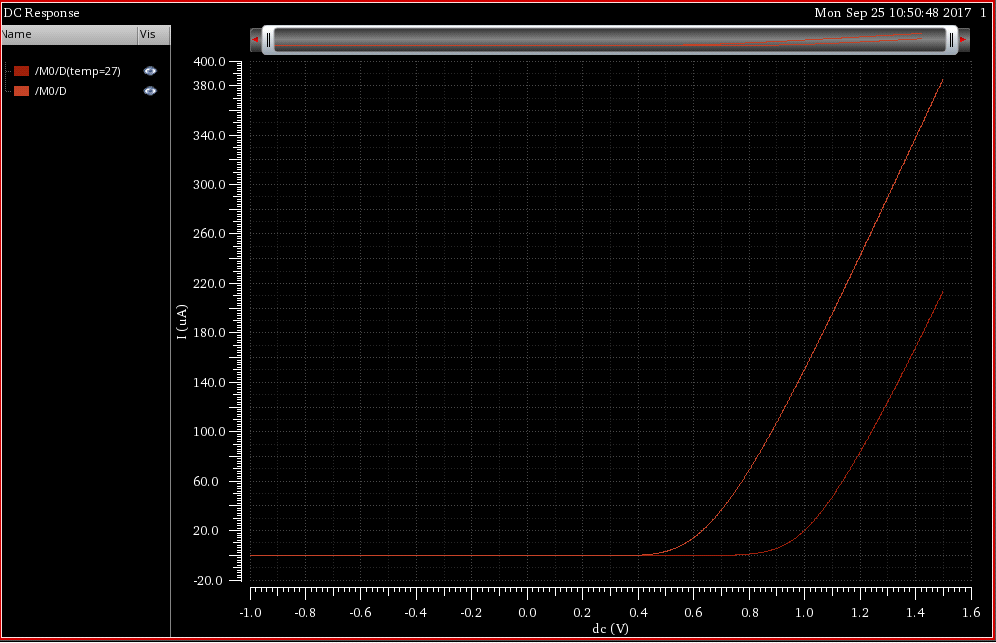
Temperatur effects



*Figur 7 Temperature effect on a NMOS transistor shown with 5 graphs between -40 and 125 degrees, blue line is at -40 degrees and the red line is at 125 degrees*

In the temperature sweep of the NMOS transistor with Vgs=0. You can see in the graph on Figur 6 that the Ioff increases when the temperature raises. Also we see that the largest effect the temperature has is in the region around Vt, where the spread is the largest between the temparatures before the saturation region.

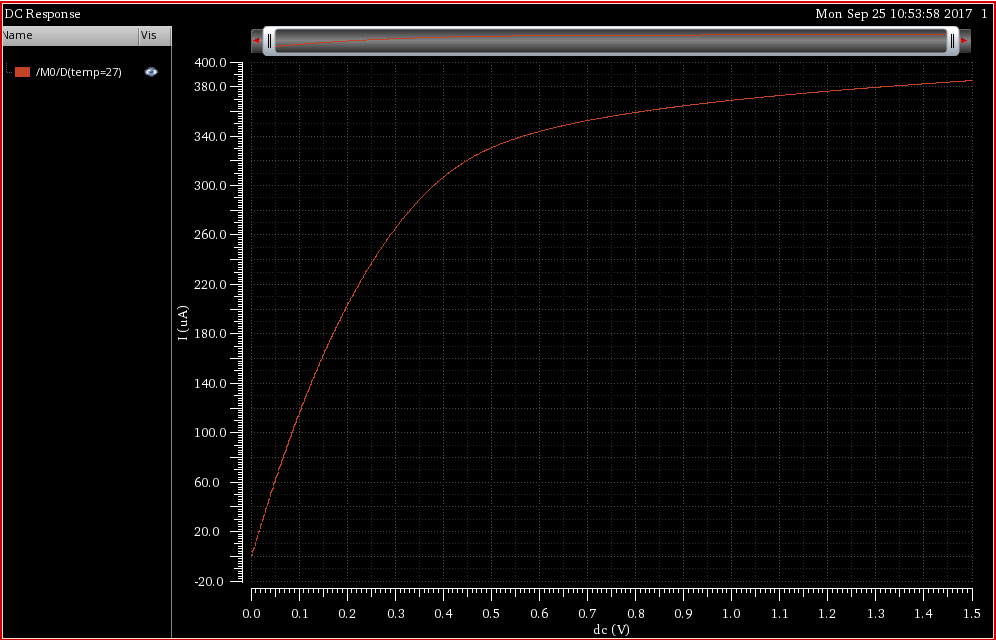
Body voltage effect on threshold voltage



*Figur 8 Threshold voltage increased after the Body is connected to Vdd instead of gnd*

By increasing the body voltage we can manipulate the threshold voltage of the transistor. As seen in Figur 9 the threshold voltage is increased to 860mVcompared to the ~560 we had before, when the bulk gate is connected to Vdd instead of gnd.

Channel length modulation coefficient

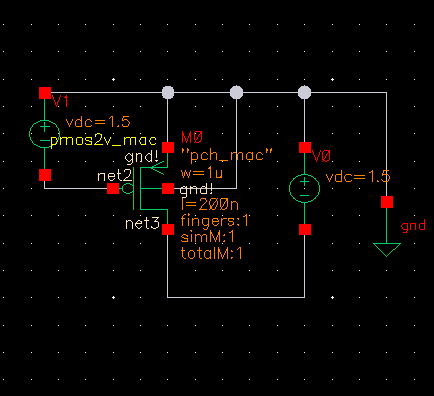


*Figur 9 Graph of the Nmos transistors Ids-Vds characteristics*

To find the Channel length modulation coefficient we follow the equation I\_dsat/R\_on, both of these can be found on the graph. I\_dsat is the current when the transistor enters the saturation region, read as the current when the voltage is at Vt. R\_on is the slope of the linear region after the transistor enters the saturation region. Reading the graph and substituting into our equation we get a Channel length modulation coefficient of: 0.118

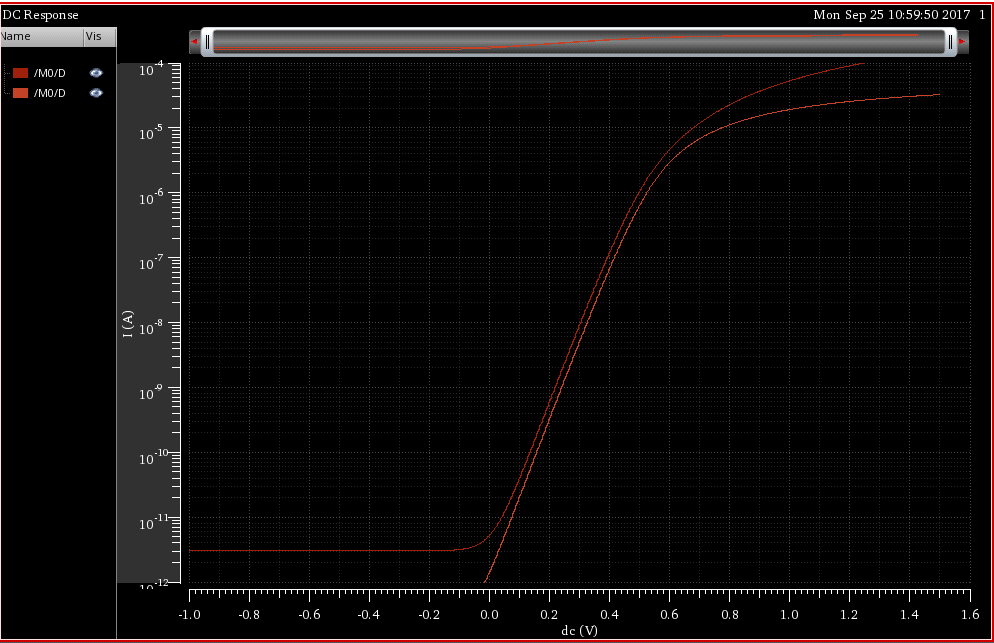
* Pmos

The Pmos transistor follows the specificationsas the Nmos; W/L=1μm/200nm and have a Vdd=1.5V. Below is the schematic of the transistor used in our simulations. for many of the parameters, the same method used for a Nmos transistor applies to the Pmos transistor as well, in these cases we will simply write the final equation or value, while refering to the Nmos section for explanations.



*Figur 10 Schematic of the Pmos transistor*

Subthreshold slope



*Figur 11 Subthreshold slope of the PMOS transistor*

The subthreshold slope of the Pmos is(see Nmos scetion for definition): 90mV/Dec

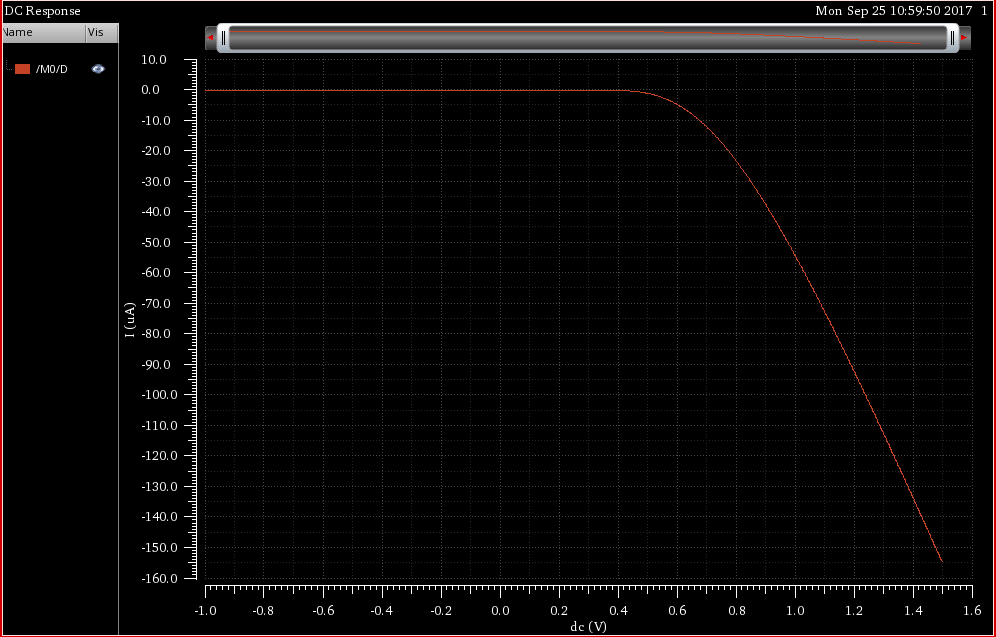
DIBL

The DIBL(Drain-Induced Barrier Lowering) of the Pmos is(see Nmos scetion for definition):: 16.9mV

Ioff

The Ioff current of the Pmos is(see Nmos scetion for definition): -5.33pA

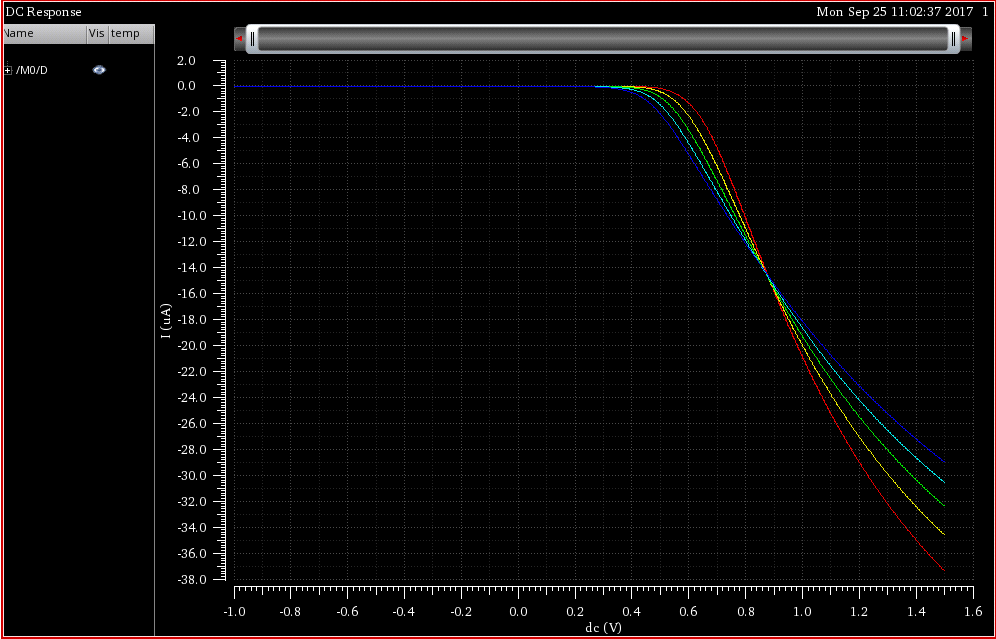
Threshold Voltage



*Figur 12 Threshold voltage of the PMOS transistor*

reading the threshold voltage is a bit different for the Pmos graph, here you need to find the point the graph enters the saturation region, or more specifik where the graph becomes linear and read the voltage value at this point. We read the Threshold voltage to be: 0.49 V

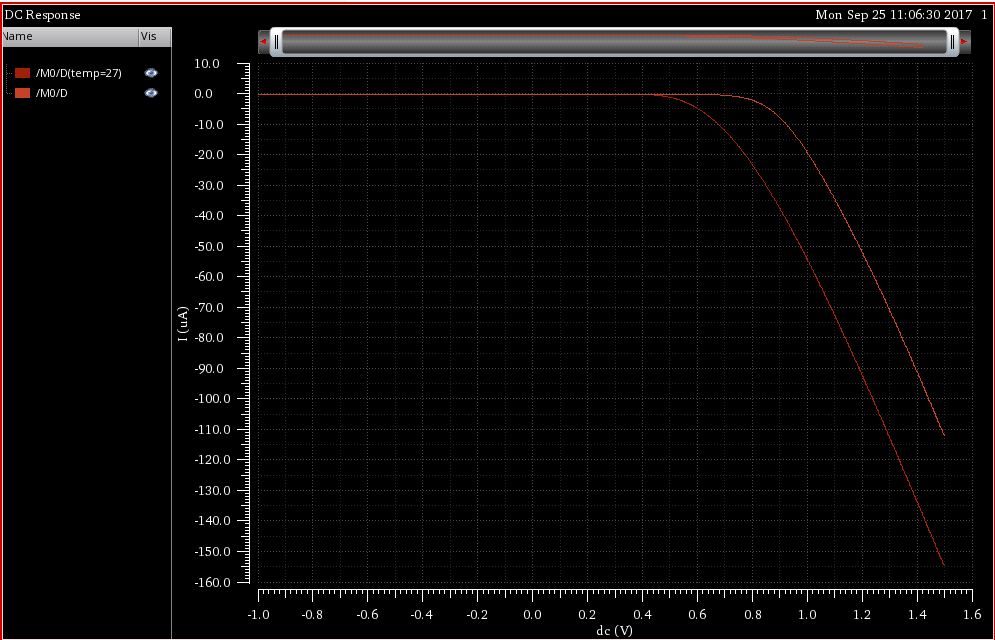
Temperatur effects



*Figur 12 Temperature effect on a PMOS transistor shown with 5 graphs between -40 and 125 degrees, blue line is at -40 degrees and the red line is at 125 degrees*

Again this graph looks different from the Nmos graph, however it shows the same effect and tendencies in increasing the spread around Vt after changing the temperature.

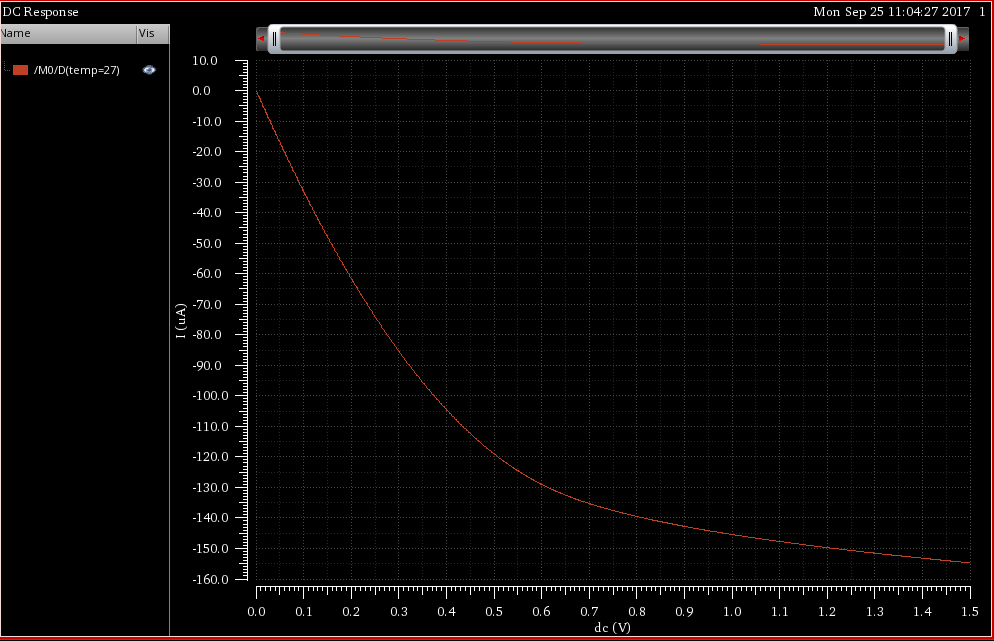
Body voltage effect on threshold voltage



*Figur 13 Threshold voltage increased after the Body is connected to Vdd instead of gnd*

By increasing the body voltage we can manipulate the threshold voltage of the transistor. As seen in Figur 13 the threshold voltage is increased to 800mVcompared to the ~560 we had before, when the bulk gate is connected to Vdd instead of gnd.

Channel length modulation coefficient



*Figur 14 Graph of the Nmos transistors Ids-Vds characteristics*

To find the Channel length modulation coefficient we follow the equation I\_dsat/R\_on, both of these can be found on the graph. I\_dsat is the current when the transistor enters the saturation region, read as the current when the voltage is at Vt. R\_on is the slope of the linear region after the transistor enters the saturation region. Reading the graph and substituting into our equation we get a Channel length modulation coefficient of: